EXAMINER AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Bhavani Rayaprolu (Reg. No. 56,583) on 13 January 2011.

3. Pursuant to MPEP 606.01, the title has been amended to read:

-- SKIPPING NON-TIME-CRITICAL TASK ACCORDING TO CONTROL TABLE WHEN OPERATING FREQUENCY FALLS --.

4. **This listing of claims will replace all prior versions and listings of claims in the application:**

1. (Currently Amended) A method of executing tasks comprising:

dividing a unit of processing time for executing tasks of a process by a processor into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks; and

skipping a task to be executed in the non-reserved band when operating frequency ~~a throughput~~ of a processor falls, wherein

a non-time-critical task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

2. (Previously Presented) The method of executing tasks according to claim 1, wherein the operating frequency of the processor is lowered when the processor or a peripheral circuit thereof exceeds a predetermined threshold in temperature.

3. (Previously Presented) The method of executing tasks according to claim 1, wherein the operating frequency of the processor is lowered depending on power consumption of the processor.

4. (Currently Amended) A task management method comprising:

classifying tasks to be executed by a processor into a first type and a second type depending on properties thereof; and

executing tasks of the first type while skipping a task of the second type to be executed between the tasks of the first type when operating frequency of the processor falls ~~if there is a possibility that time-critical timeness of processing is impaired by a predetermined factor~~, wherein

the second type of task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of the second type of task to be executed at the operating frequency. ~~which determines how far to execute the second type of tasks in association with each other.~~

5. (Currently Amended) The task management method according to claim 4, wherein:

the processor recognizes, by a predetermined method, that a [[the]] task of the first type is one that is time-critical; and

the processor recognizes, by a predetermined method, that a [[the]] task of the second type is one that is non-time-critical.

6. (Currently Amended) A task management device comprising:

a local memory;

a switch instruction unit, which issues an instruction to switch a plurality of tasks to be executed by a main processing unit; and

a detection unit, which detects operating frequency ~~the throughput~~ of the main processing unit ~~processor~~, wherein the switch instruction unit divides a unit of processing time of processing into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks, and skips a task to be executed in

the non-reserved band when the operating frequency ~~a throughput~~ of the main processing unit falls, ~~and~~ wherein

a non-time-critical task is determined to be skipped by consulting a control target table stored in memory, wherein the control target table stores information on operating frequency of the main processing unit and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

7. (Canceled)

8. (Currently Amended) The task management device according to claim 6, further comprising an interpretation unit, which interprets a [[the]] time-critical requirement pertaining to programs executed by the respective tasks, and wherein

the switch instruction unit allocates each of the tasks to either the reserved band or the non-reserved band based on the interpretation.

9. (Previously Presented) The task management device according to claim 6, further comprising a determination unit that determines properties of programs executed by the respective tasks, and wherein

the switch instruction unit allocates each of the tasks to either the reserved band or the non-reserved band based on the determination.

10. (Previously Presented) The task management device according to claims 6, wherein the unit of processing time is one pertaining to display processing.

11-12. (Canceled)

13. (Currently Amended) A task management device comprising:

a local memory;

a switch instruction unit, which issues an instruction to switch a plurality of tasks to be executed by a main processing unit; and

a detection unit, which detects operating frequency ~~the throughput~~ of the main processing unit, wherein

the switch instruction unit classifies the tasks to be executed by the main processing unit into a first type and a second type depending on properties thereof, and executes tasks of the first type while skipping a task of the second type to be executed between the tasks of the first type when operating frequency of the main processing unit falls ~~if there is a possibility that time-critical processing is impaired by a predetermined factor~~, wherein

the second type of task is determined to be skipped by consulting a control target table stored in memory, wherein the control target table stores information on operating frequency of the main processing unit and an associated rate of execution of the second type of task to be executed at the operating frequency. ~~which determines how far to execute the second type of tasks in association with each other.~~

14. (Currently Amended) A semiconductor integrated circuit comprising:

a main processing unit, which executes predetermined tasks; and

a task management unit, which divides a unit of processing time of processing into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks, and skips a task to be executed in the non-reserved band when operating frequency ~~a throughput~~ of the main processing unit falls,

a non-time-critical task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the main processing unit and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

15. (Currently Amended) The semiconductor integrated circuit according to claim 14, further comprising a clock generation unit, which supplies a clock having a predetermined operating frequency to the main processing unit. ~~, and wherein~~

~~the task management unit skips a task to be executed in the non-reserved band as appropriate when the operating frequency falls.~~

16. (Original) The semiconductor integrated circuit according to claim 15, wherein the clock generation unit lowers the operating frequency when the main processing unit or a periphery thereof exceeds a predetermined threshold in temperature.

17. (Original) The semiconductor integrated circuit according to claim 16, wherein the clock generation unit lowers the operating frequency depending on power consumption.

18. (Previously Presented) The semiconductor integrated circuit according to claim 15, wherein the task management unit skips the task to be executed in the non-reserved band when the main processing unit or a periphery thereof exceeds a predetermined threshold in temperature.

19. (Previously Presented) The semiconductor integrated circuit according to claim 15, wherein the task management unit skips the task to be executed in the non-reserved band depending on power consumption.

20. (Currently Amended) A semiconductor integrated circuit comprising:

a main processing unit, which executes tasks at a predetermined operating frequency;

a clock generation unit, which supplies a clock having the operating frequency to the main processing unit;

a circuit, which receives a task management function for task management to divide a unit of processing time into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks for skipping a task to be executed in

the non-reserved band when the operating frequency of the main processing unit ~~a processor~~ falls; and

a control target table, wherein a non-time-critical task is determined to be skipped by consulting the control target table, wherein the control target table stores information on operating frequency of the main processing unit and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

21. (Currently Amended) An electronic apparatus comprising:

a processor, which executes tasks at a predetermined operating frequency; and

a storing unit, which stores a program to be executed by said processor, wherein the processor executes the program to perform a [[the]] function for task management to divide a unit of processing time into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks for skipping a task to be executed in the non-reserved band when the operating frequency of the [[a]] processor falls; and

a control target table, wherein a non-time-critical task is determined to be skipped by consulting the control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

22. (Original) The electronic apparatus according to claim 21, further comprising a frequency control unit which lowers the operating frequency when the processor or a peripheral circuit thereof exceeds a predetermined threshold in temperature.

23. (Original) The electronic apparatus according to claim 21, further comprising a frequency control unit which lowers the operating frequency depending on power consumption.

24. (Currently Amended) A computer-readable storage medium that stores a program executed by a processor, the program including a [[the]] function of:

dividing a unit of processing time into a reserved band for guaranteeing time-critical tasks and a non-reserved band for non-time-critical tasks for skipping a task to be executed in the non-reserved band when operating frequency ~~the throughput~~ of the processor falls,

wherein a non-time-critical task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

25. (Currently Amended) A computer-readable storage medium that stores a program executed by a processor, the program including the functions of:

classifying tasks to be executed by the processor into a first type and a second type depending on properties thereof; and

executing tasks of the first type while skipping a task of the second type to be executed between the tasks of the first type when operating frequency of the processor falls ~~if there is a possibility that time-critical timeness of processing is impaired by a predetermined factor~~, wherein

the second type of task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of the second type of task to be executed at the operating frequency. ~~which determines how far to execute the second type of tasks in association with each other.~~

26. (Currently Amended) A task management system comprising:

a processor, which executes tasks at a predetermined operating frequency;

a clock generation unit, which supplies a clock having the operating frequency to said processor; and

a switch instruction unit, which issues an instruction to switch a plurality of tasks to be executed by said processor, wherein

the switch instruction unit divides a unit of processing time for executing tasks of a process by the [[a]] processor into a reserved band for guaranteeing time-critical tasks

and a non- reserved band for non-time-critical tasks and skips a task to be executed in the non-reserved band when the operating frequency of the [[a]] processor falls, and wherein

a non-time-critical task is determined to be skipped by consulting a control target table, wherein the control target table stores information on operating frequency of the processor and an associated rate of execution of a task to be executed in the non-reserved band at the operating frequency. ~~which determines how far to execute non-time-critical tasks in association with each other.~~

27. (Original) The task management system according to claim 26, wherein the clock generation unit lowers the operating frequency when the processor or a peripheral circuit thereof exceeds a predetermined threshold in temperature.

28. (Original) The task management system according to claim 26, wherein the clock generation unit lowers the operating frequency depending on power consumption.

29-30. (Canceled)

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance:

Interpreting the claims in light of the specification, Examiner finds the claimed invention is patentably distinct from the prior art of record. The prior art does not

expressly teach or render obvious the invention as recited in independent claims 1,4, 6, 13-14, 20-21 and 24-26. In particular, the prior art fails to teach skipping a non-time-critical task according to a control target table when operating frequency of a processor falls, where the control target table stores information on operating frequency of the processor and an associated rate of execution of the non-time-critical task at the operating frequency.

Gomi et al. (US 5,794,036) teaches omitting execution of soft-real-time processes to ease damages on a real-time operating ability of a periodic process. Particularly, Gomi teaches omits execution of soft-real-time processes based on multivalued load levels, where frequency of executing soft-real-time processes varies based on the multivalued load levels.

Saito et al. (US 5,723,998) teaches adjusting a processor clock speed based on detected temperature or driving voltage of a processor. Rescheduling, such as removing or changing priority of a task may be carried out in response to a rise in temperature.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN CHEW whose telephone number is (571)270-5571. The examiner can normally be reached on Monday-Thursday, 8:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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